FIG. 1

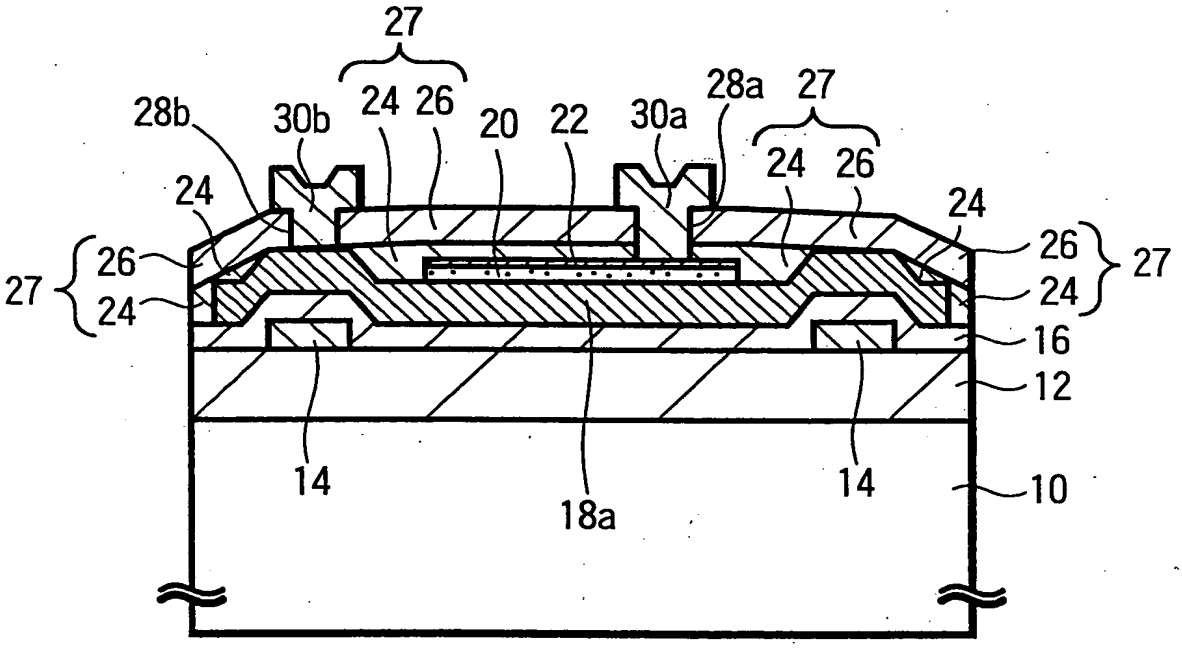
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FIG. 2

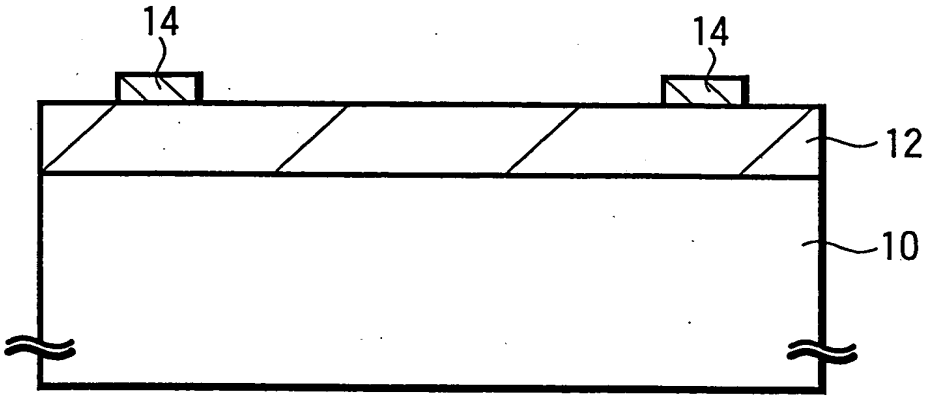

FIG. 3

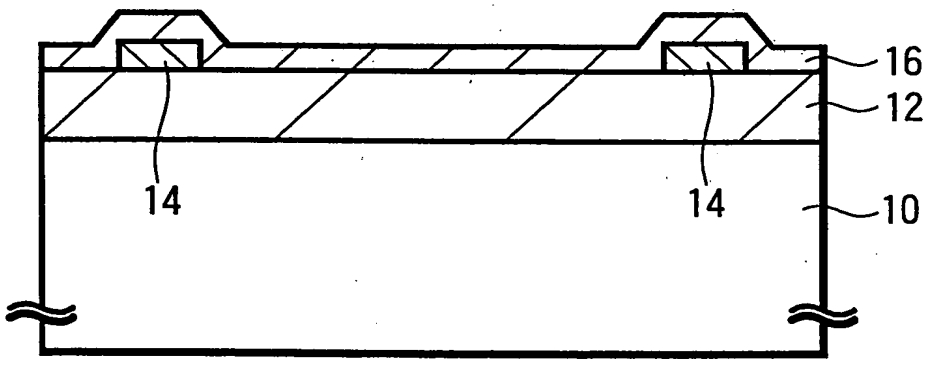

FIG. 4

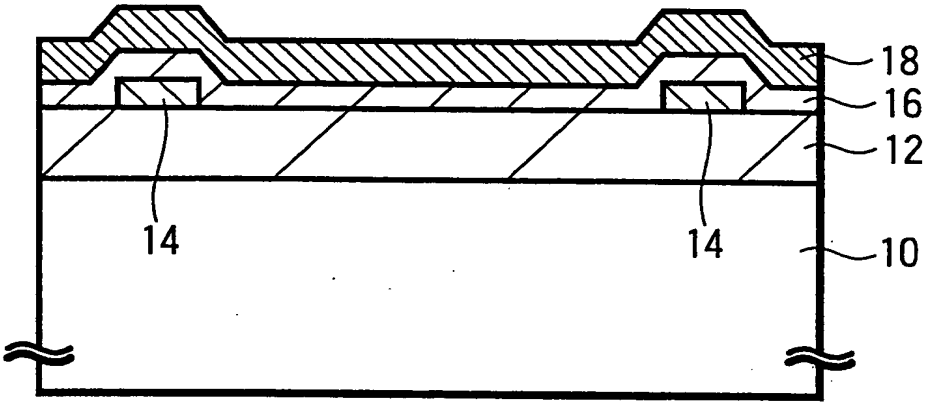

FIG. 5

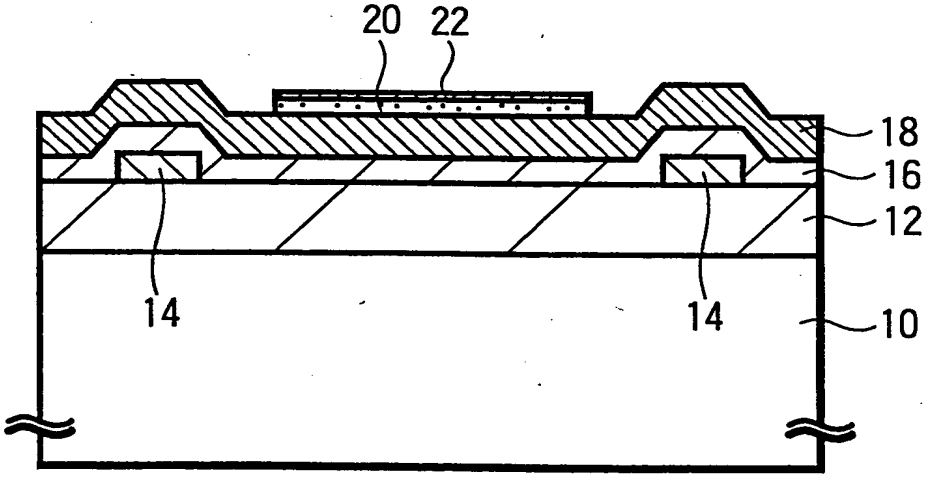

FIG. 6

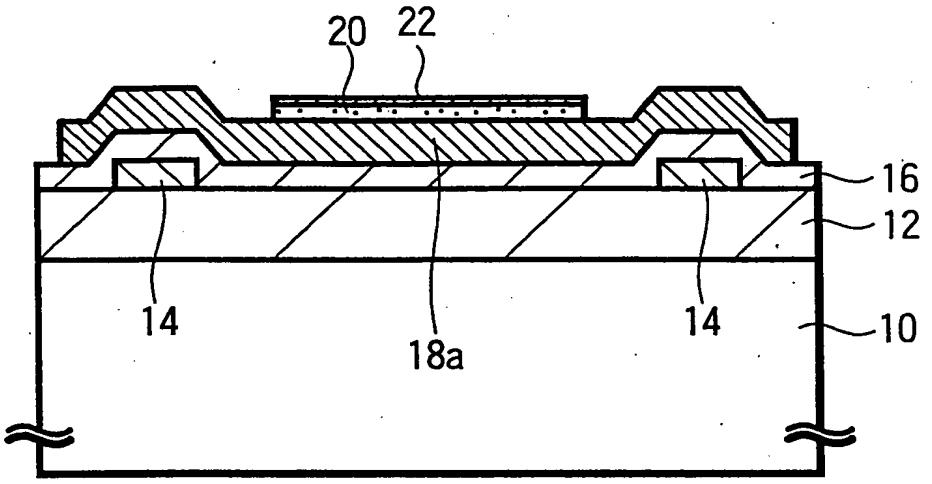

FIG. 7

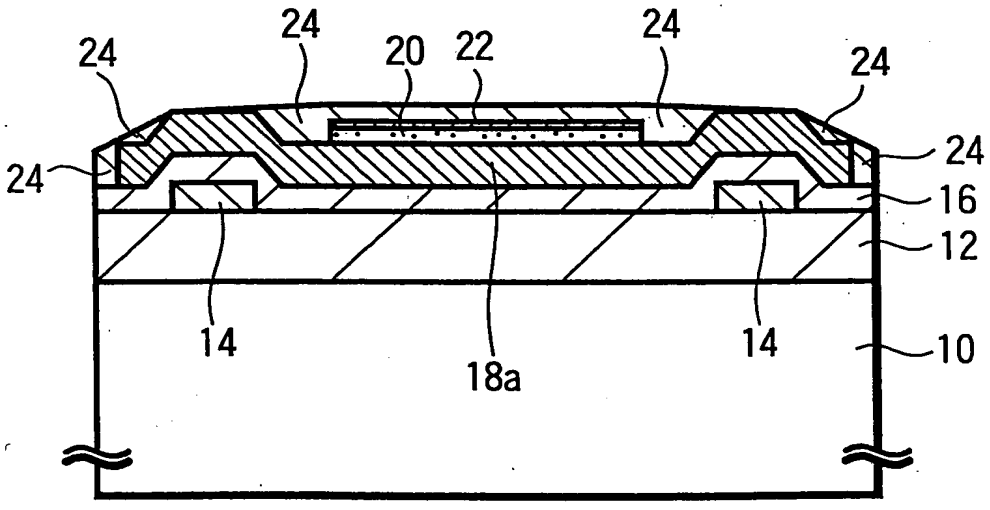

FIG. 8

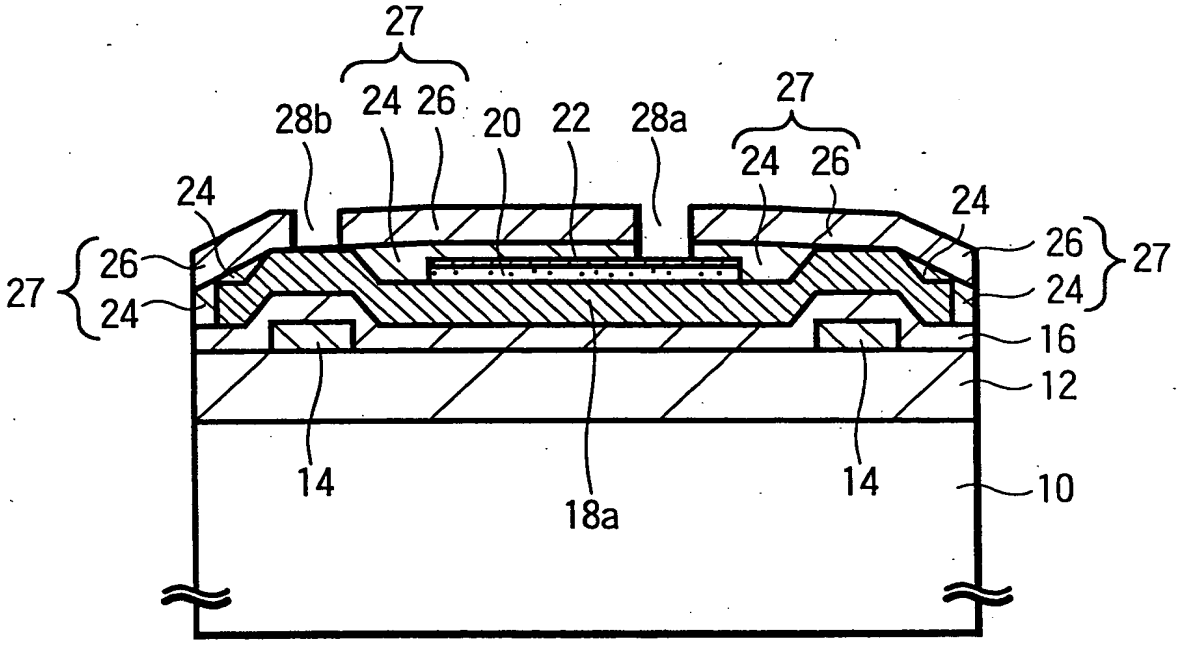
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FIG. 9

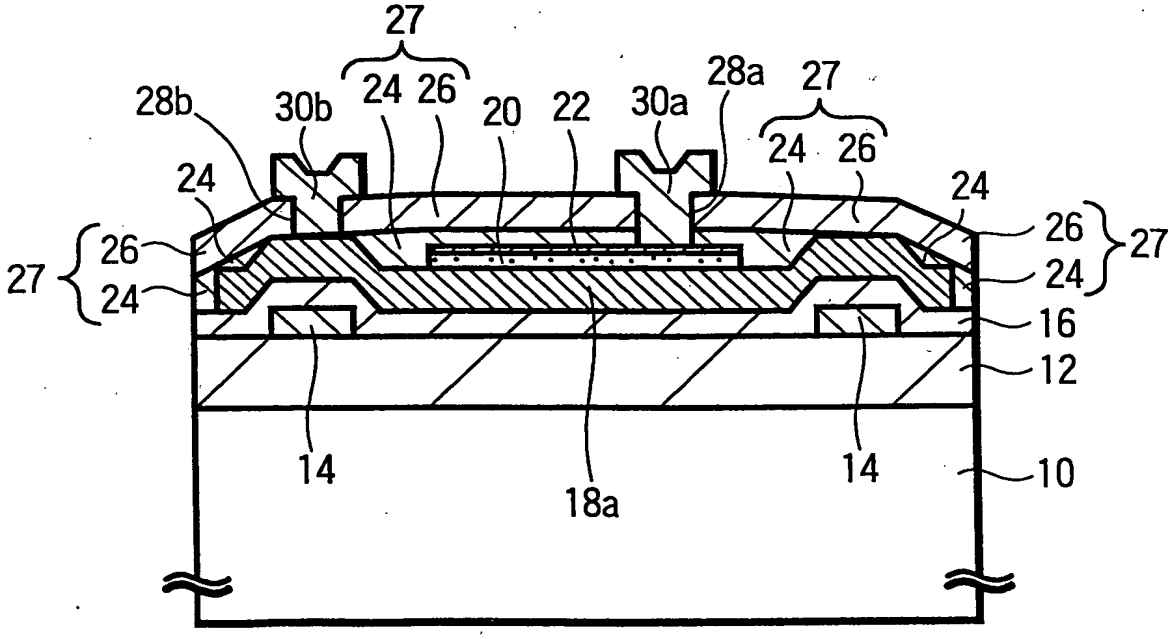
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FIG. 10

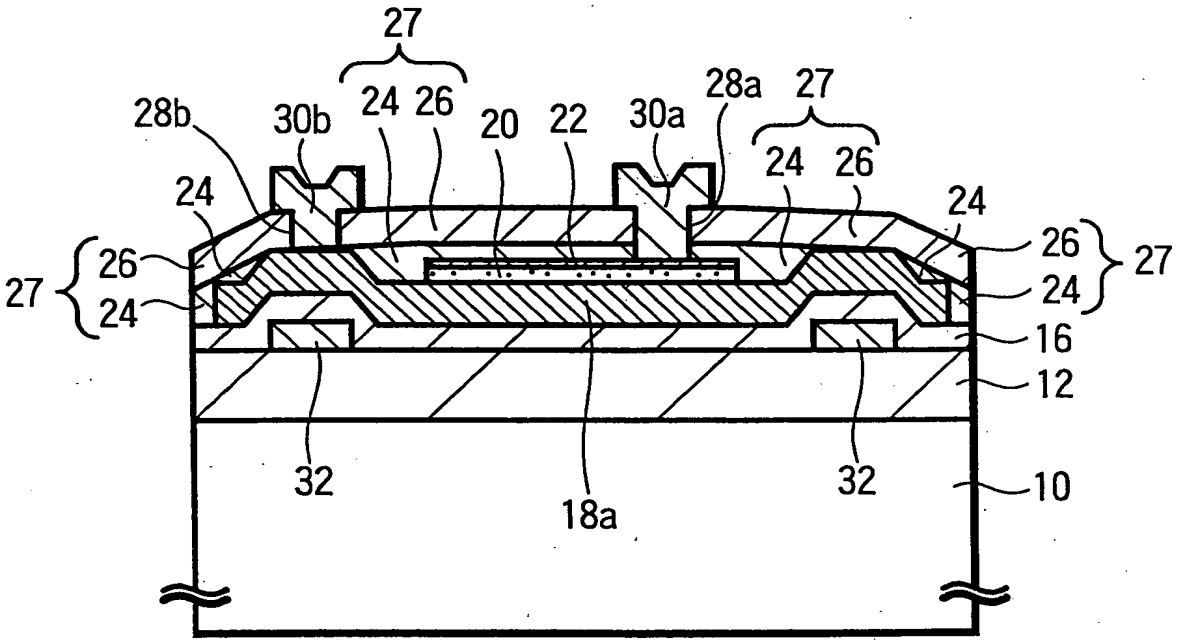
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FIG. 11

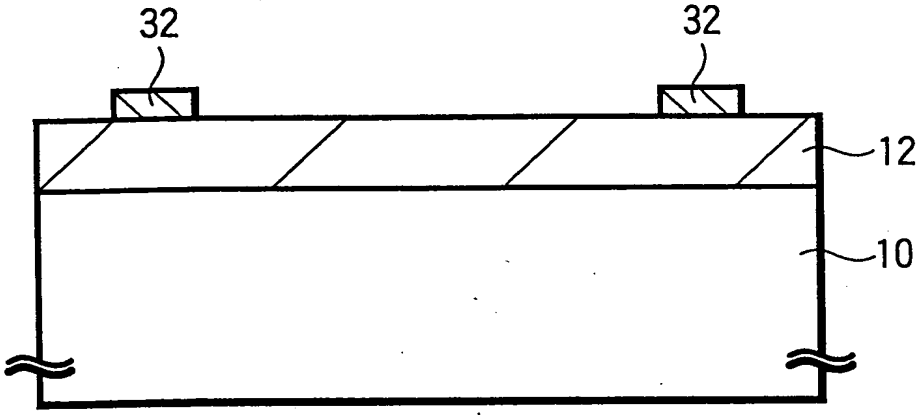
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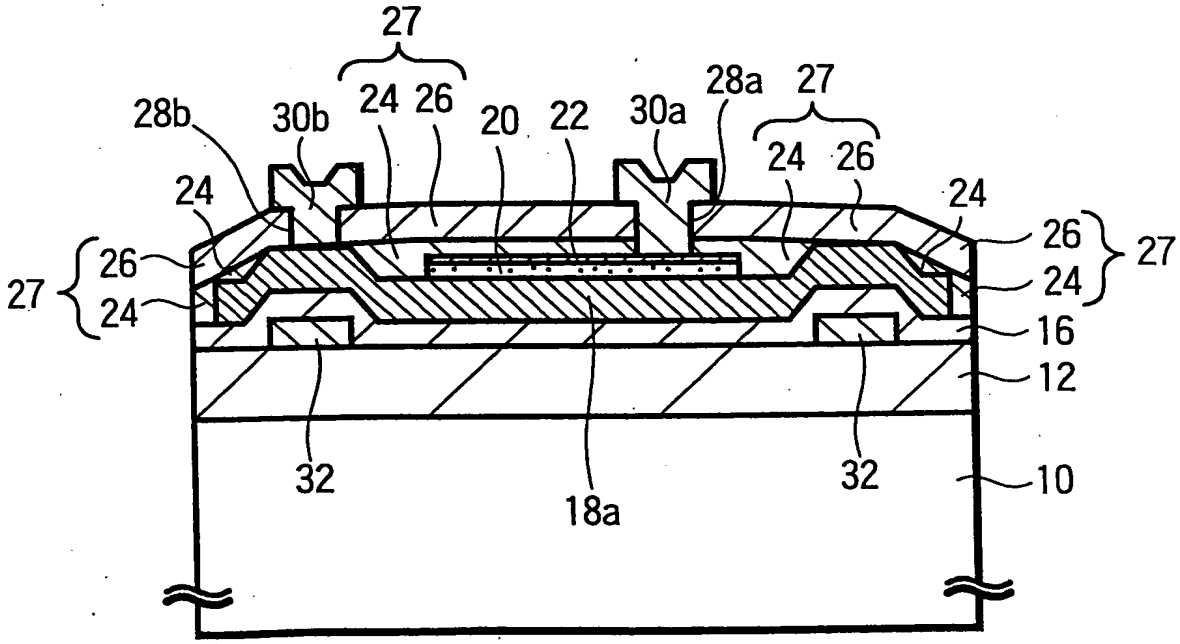
FIG. 12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18a
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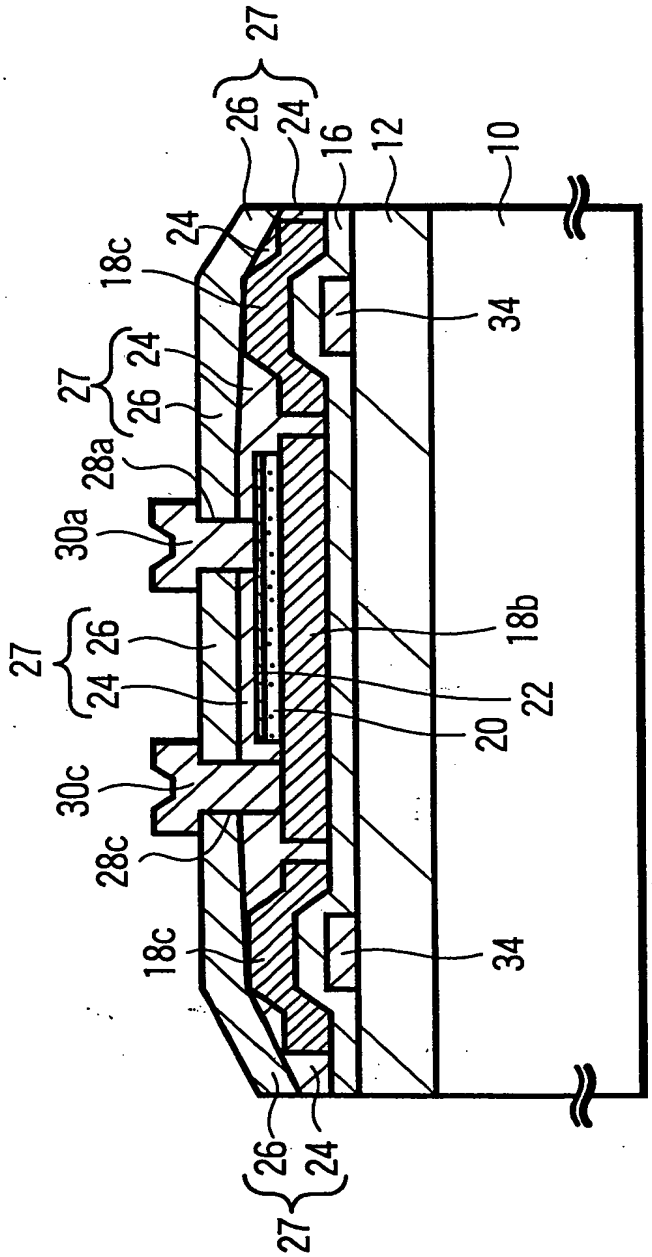
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30c
28c
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FIG. 13

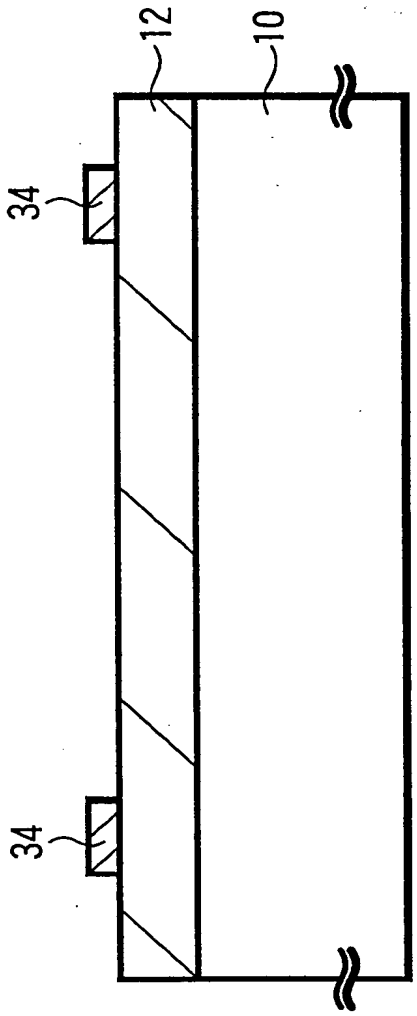


FIG. 14

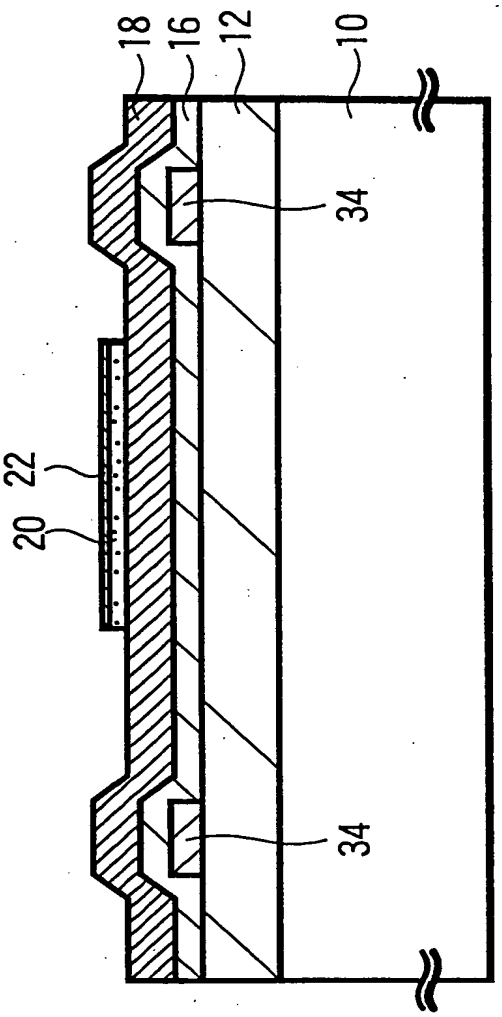
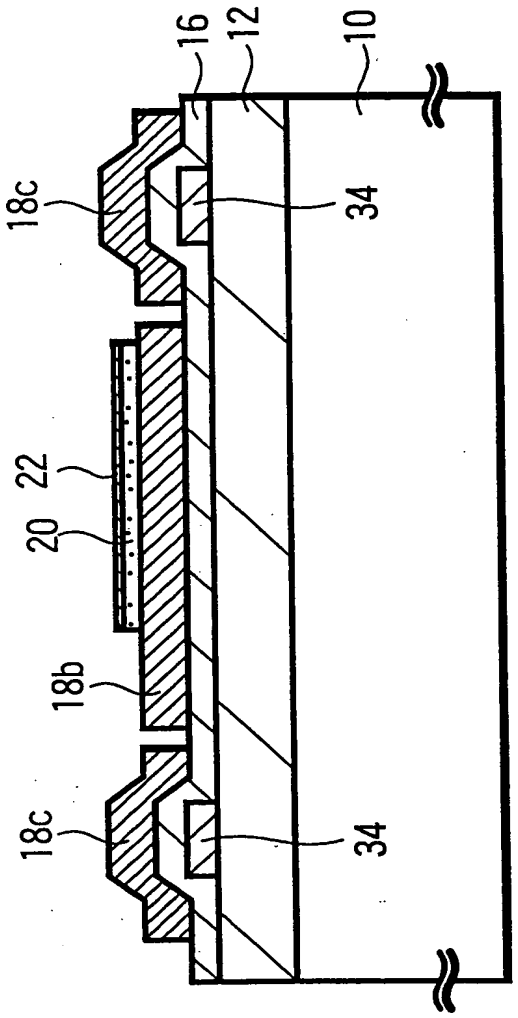


FIG. 15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18c
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18b
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FIG. 16

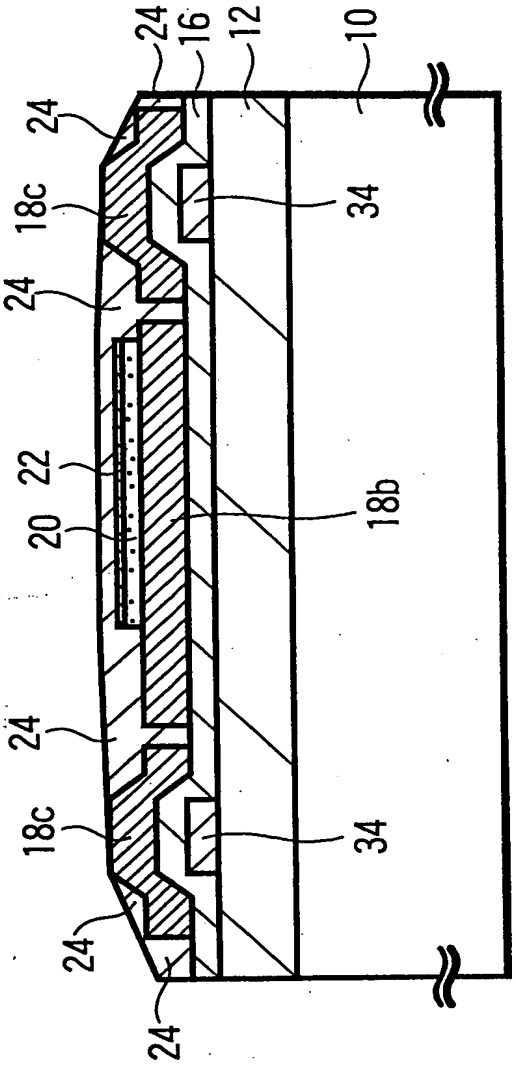
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FIG. 17

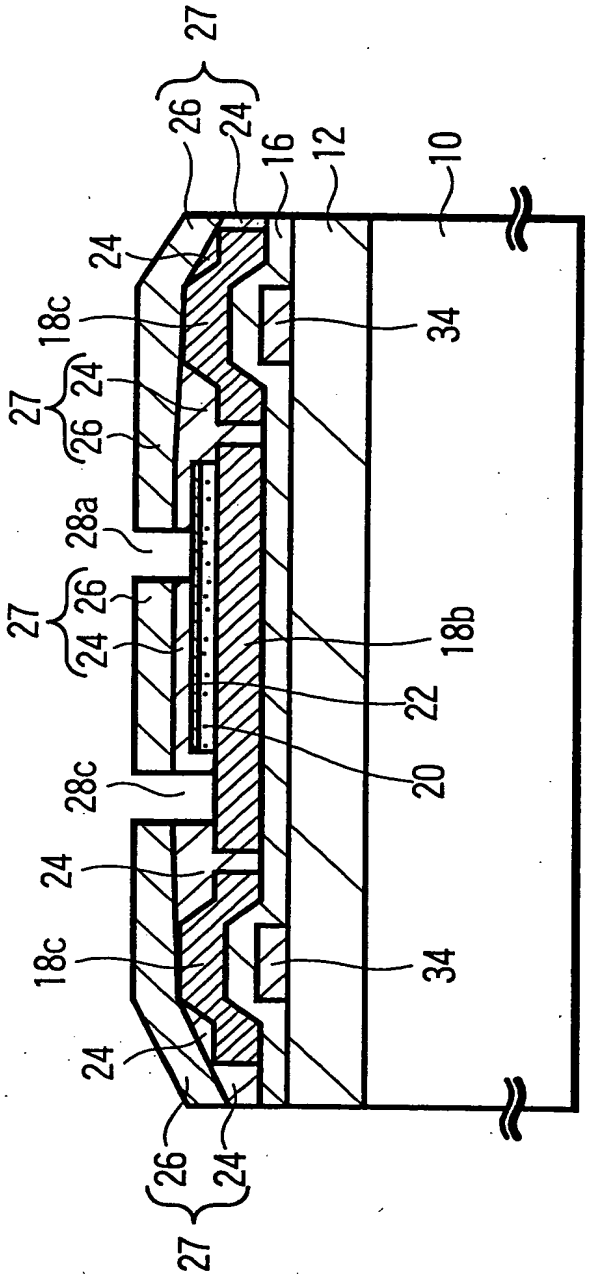
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FIG. 18

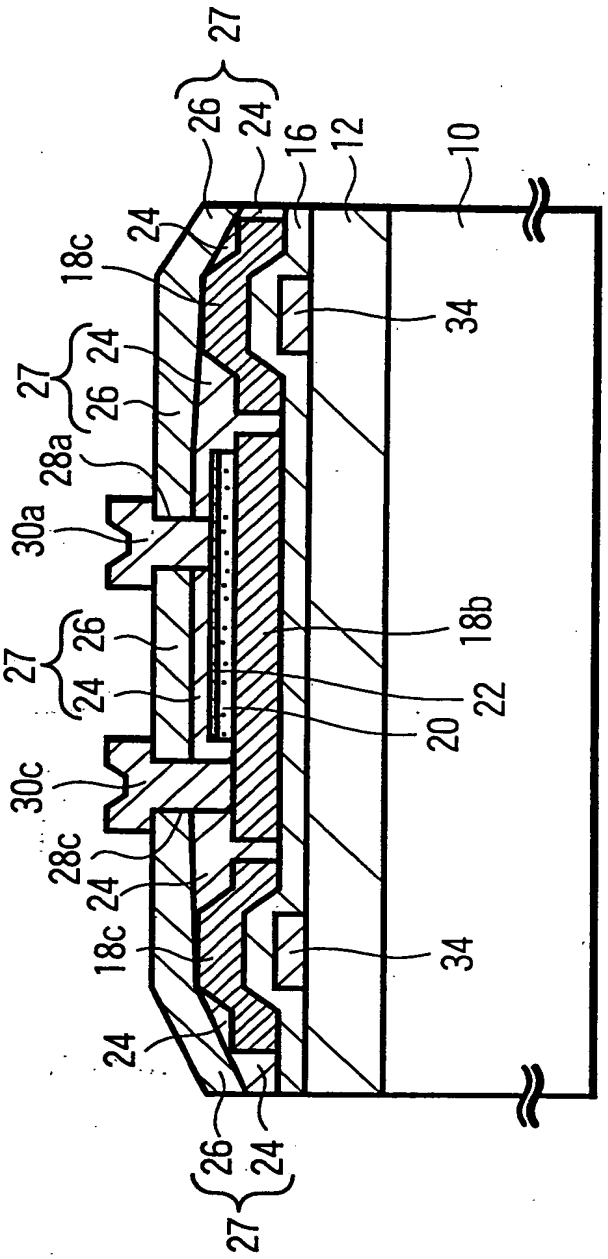
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FIG. 19

FIG. 20

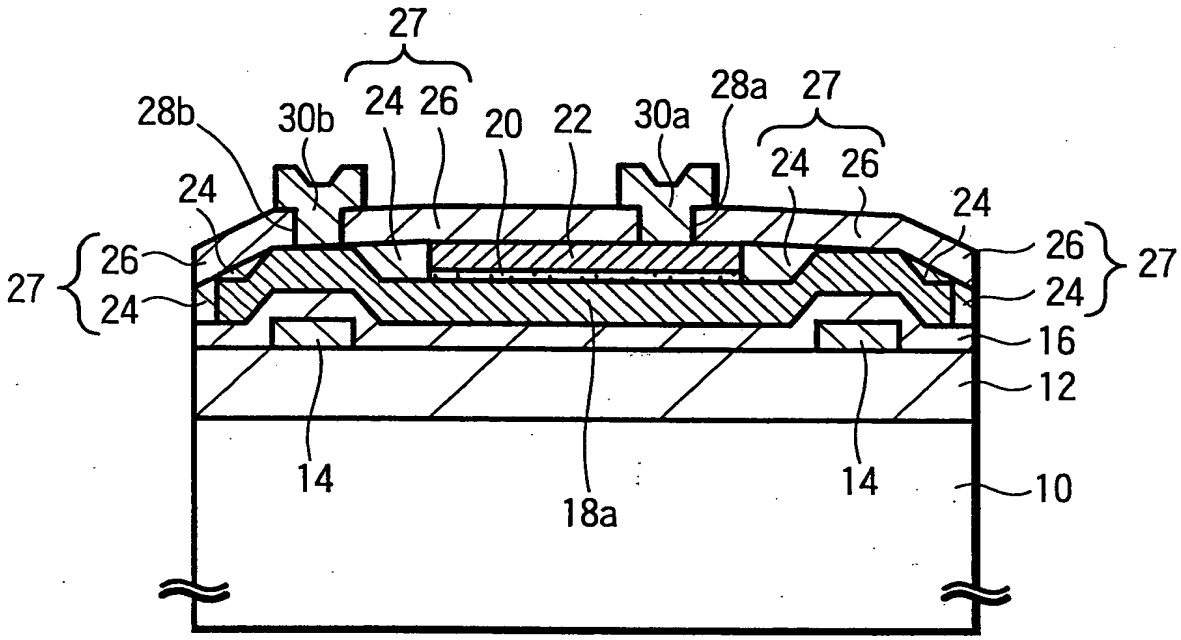
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FIG. 21

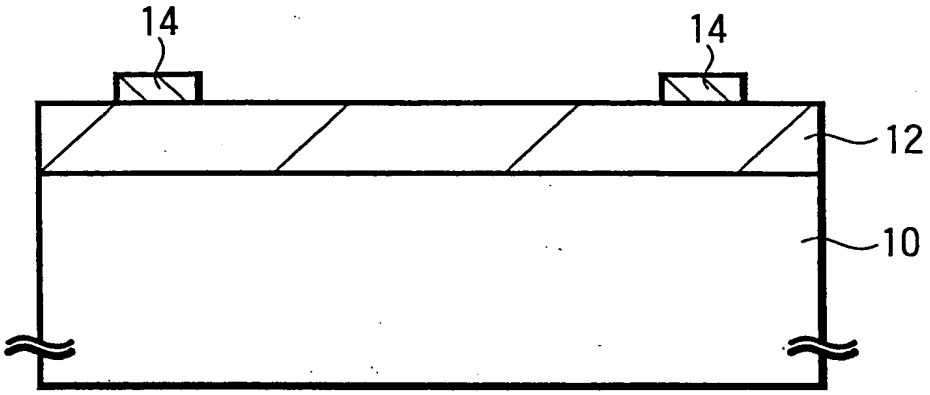

FIG. 22

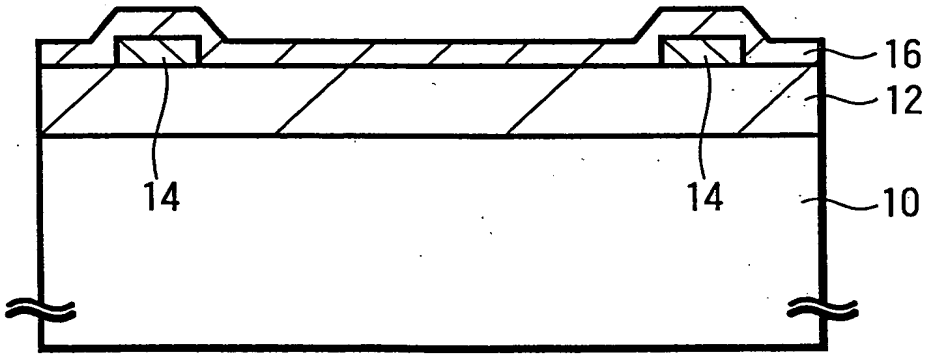

FIG. 23

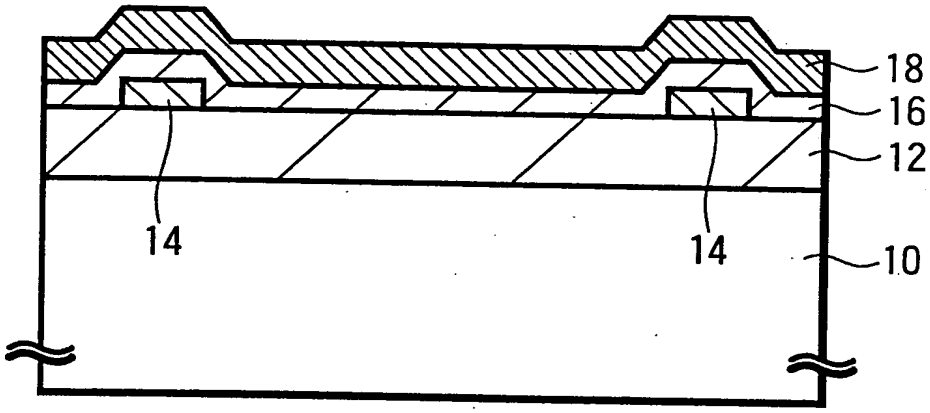

FIG. 24

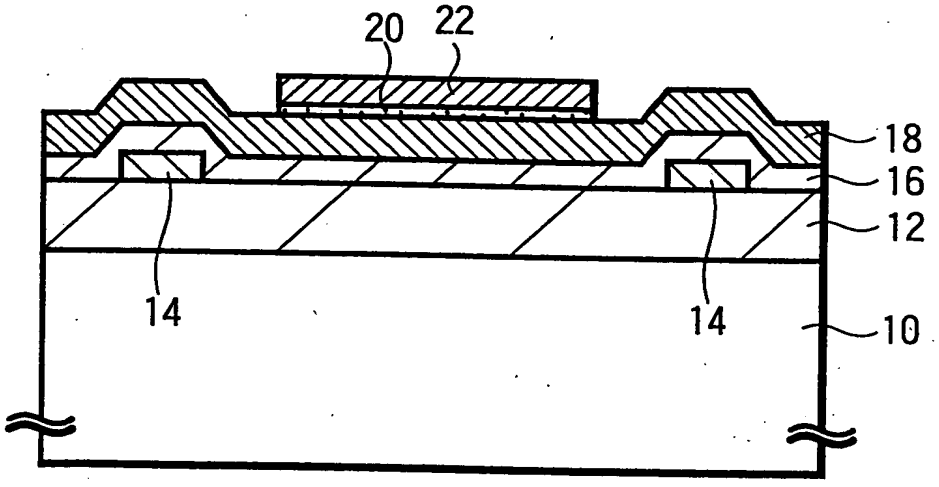

FIG. 25

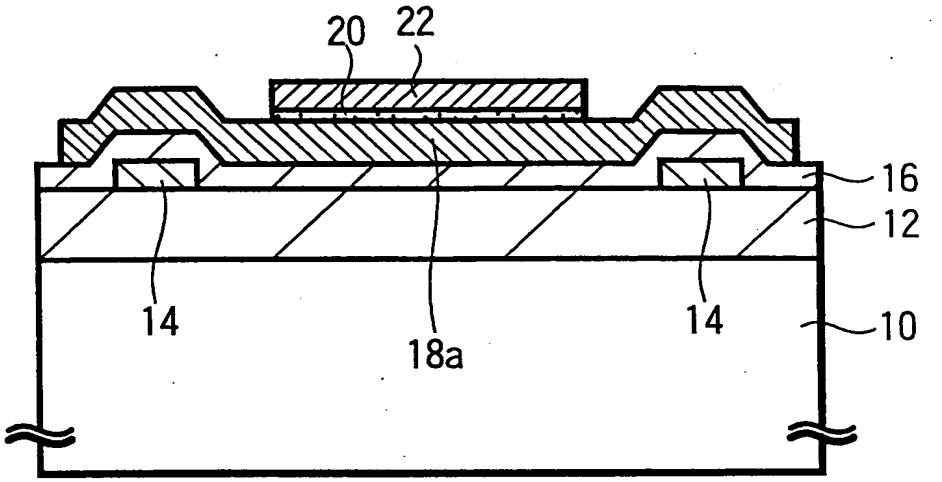

FIG. 26

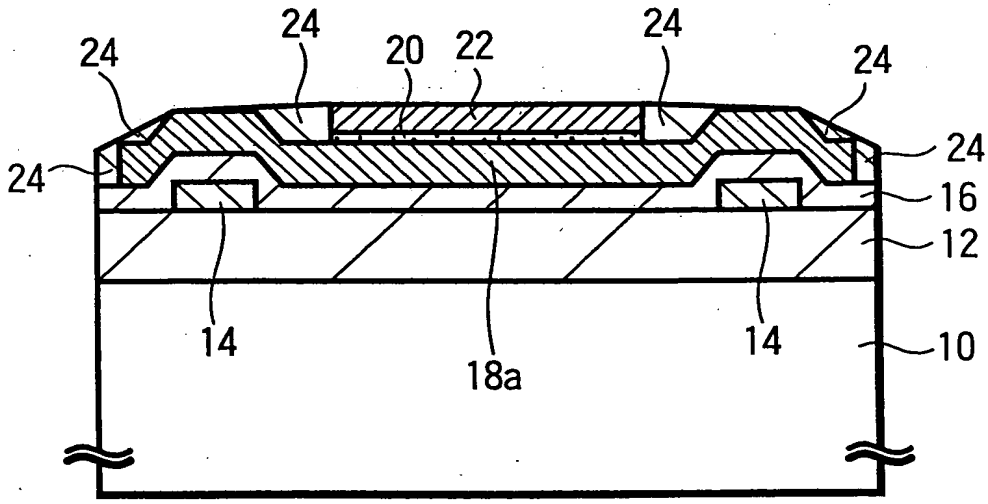

FIG. 27

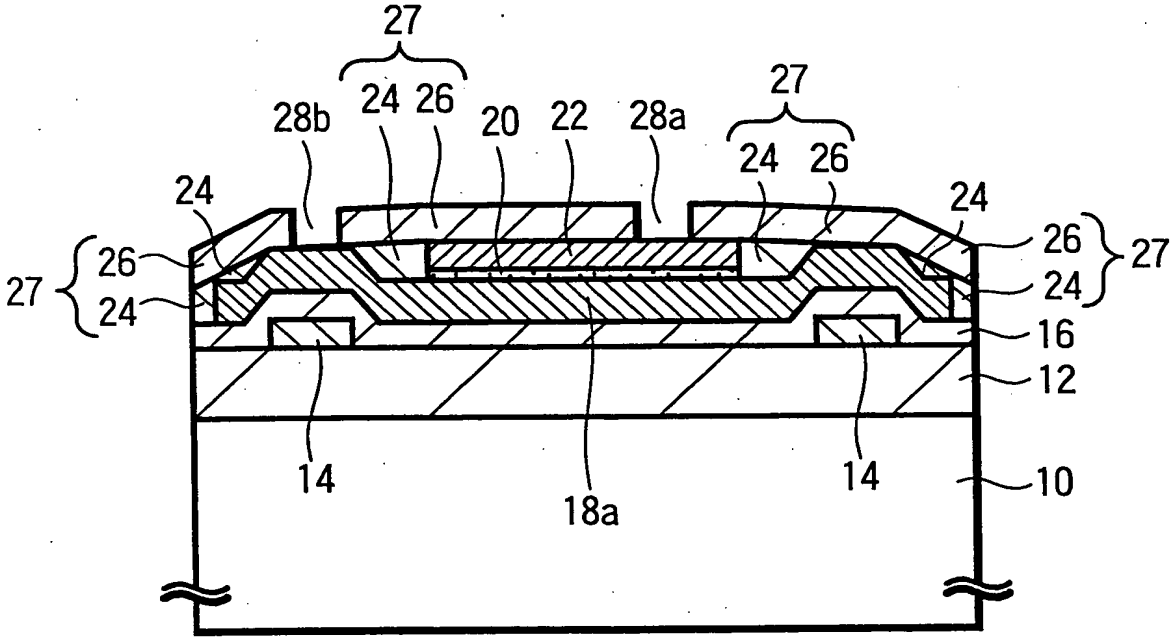
27
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FIG. 28

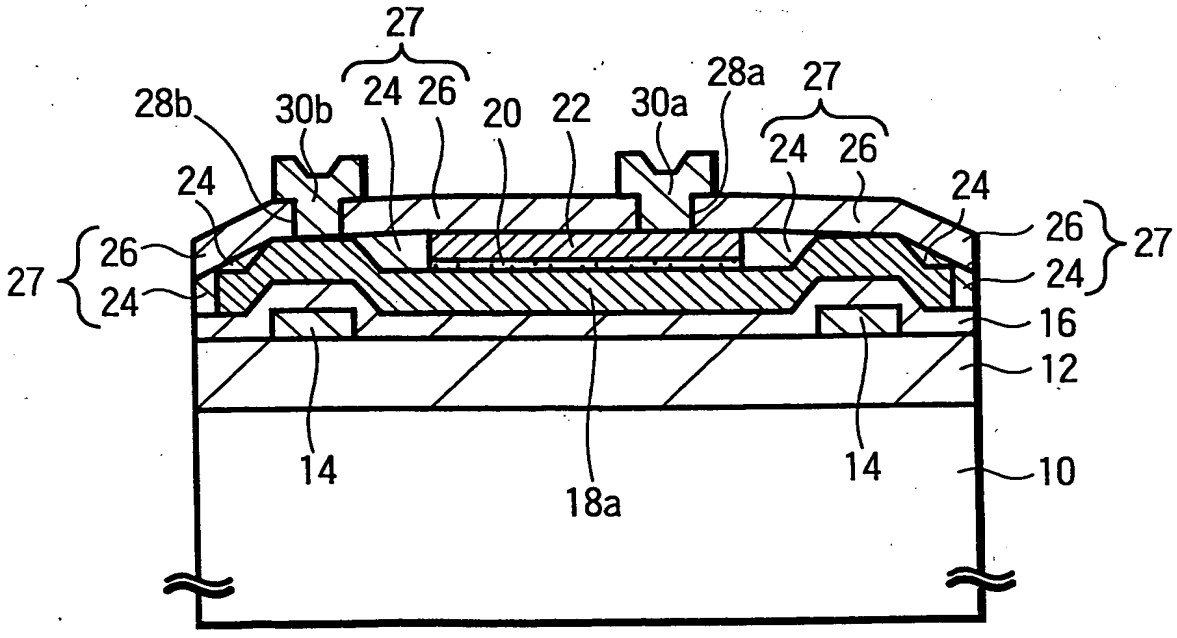
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FIG. 29

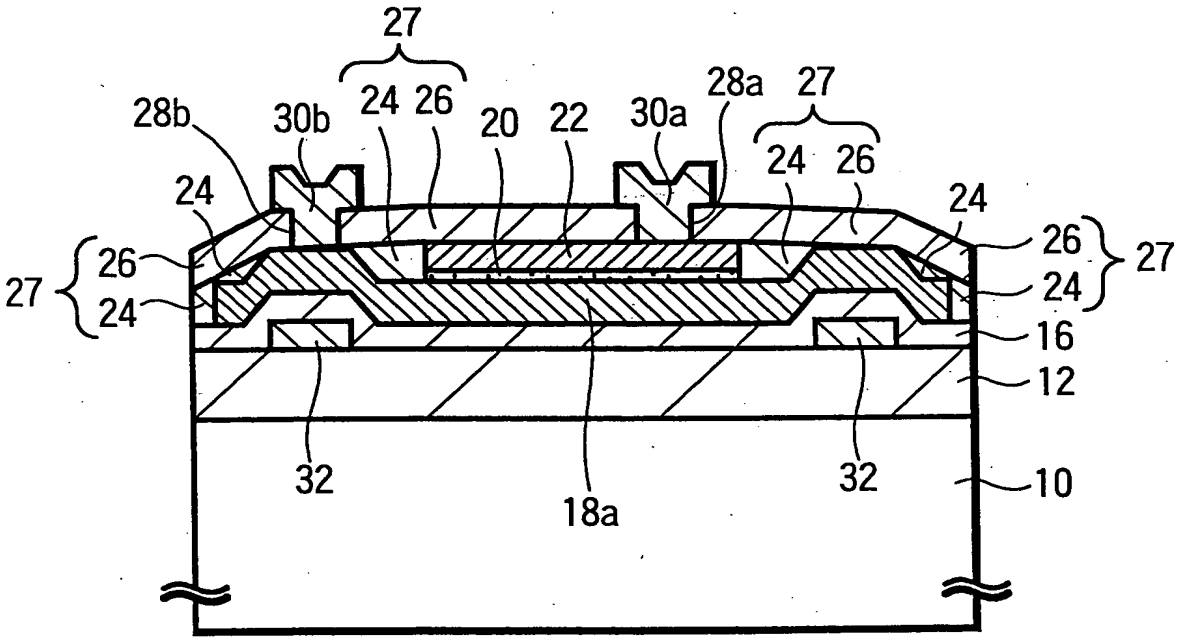
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FIG. 30

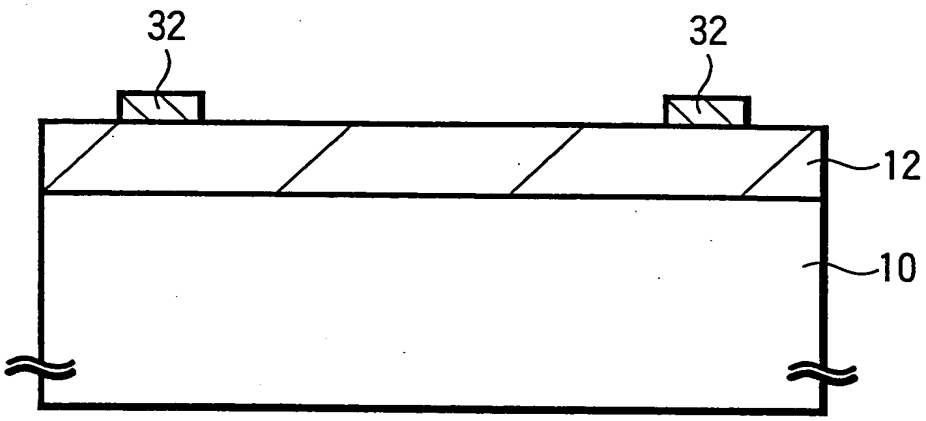
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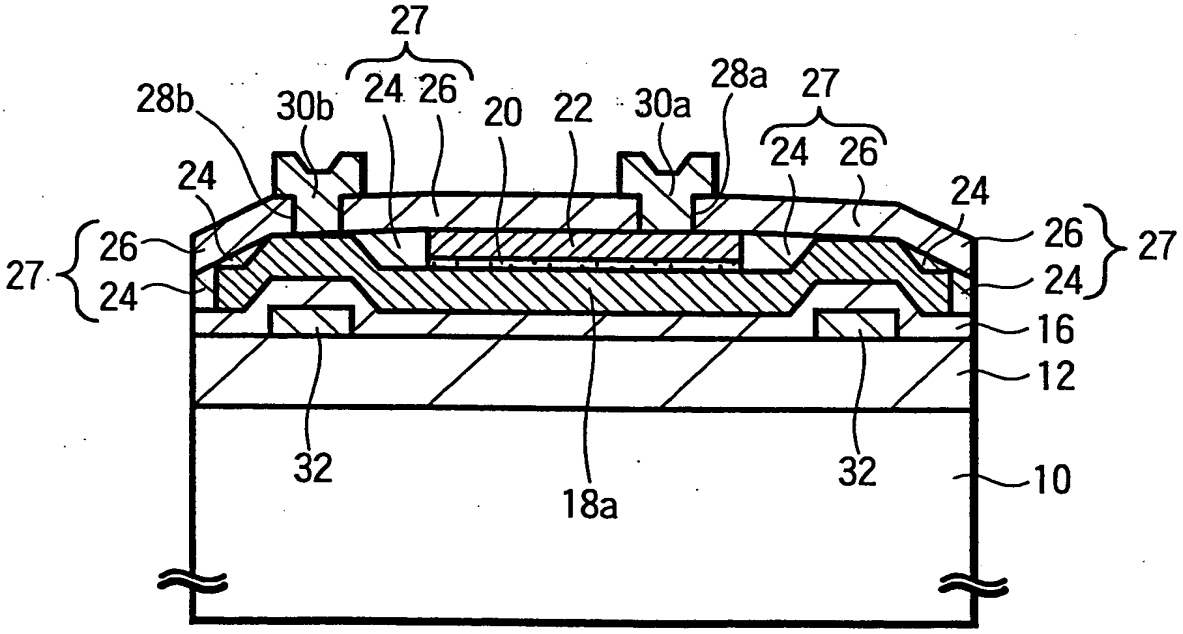
FIG. 31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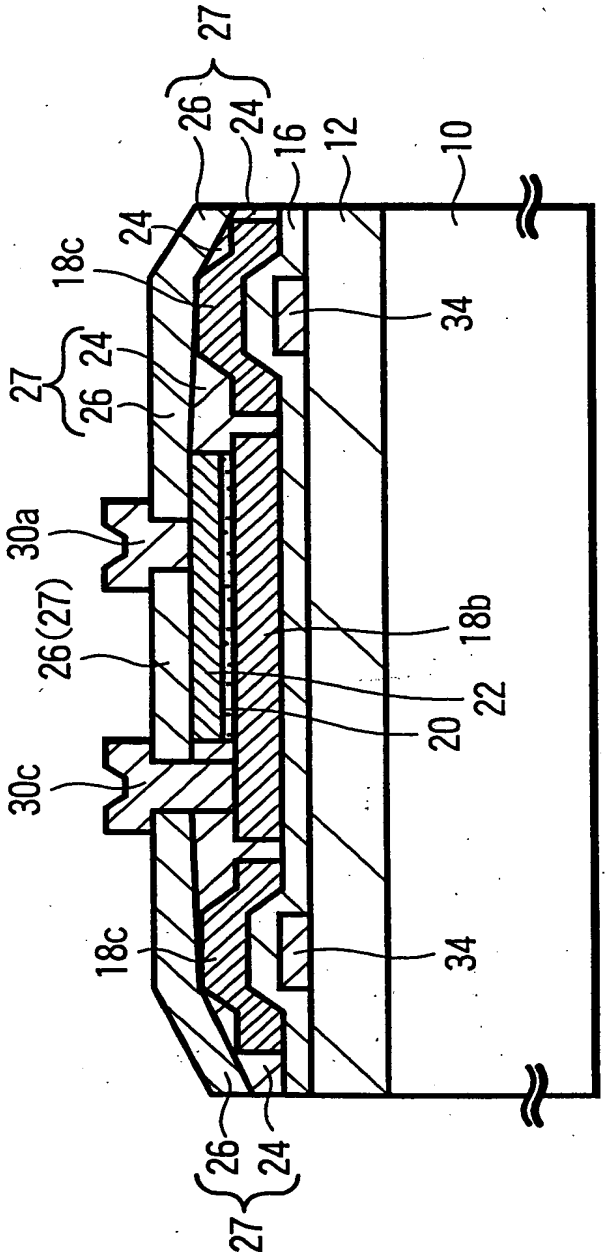
27
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18c
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FIG. 32

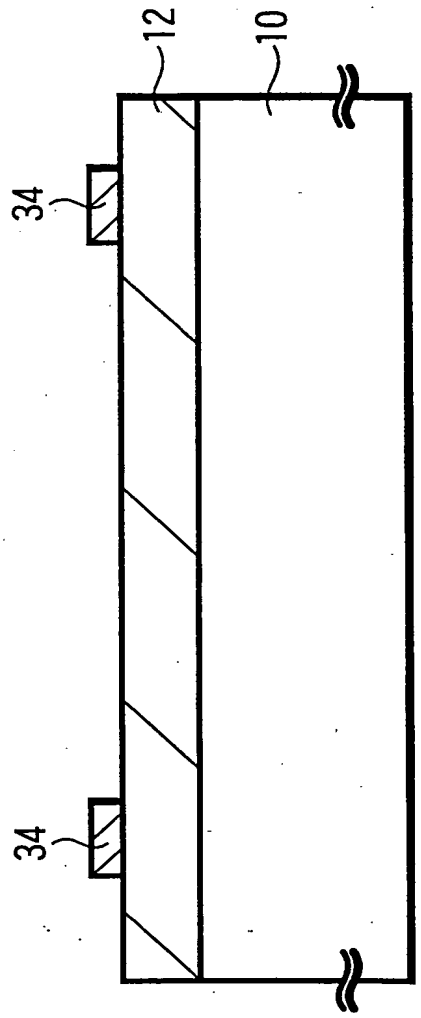

FIG. 33

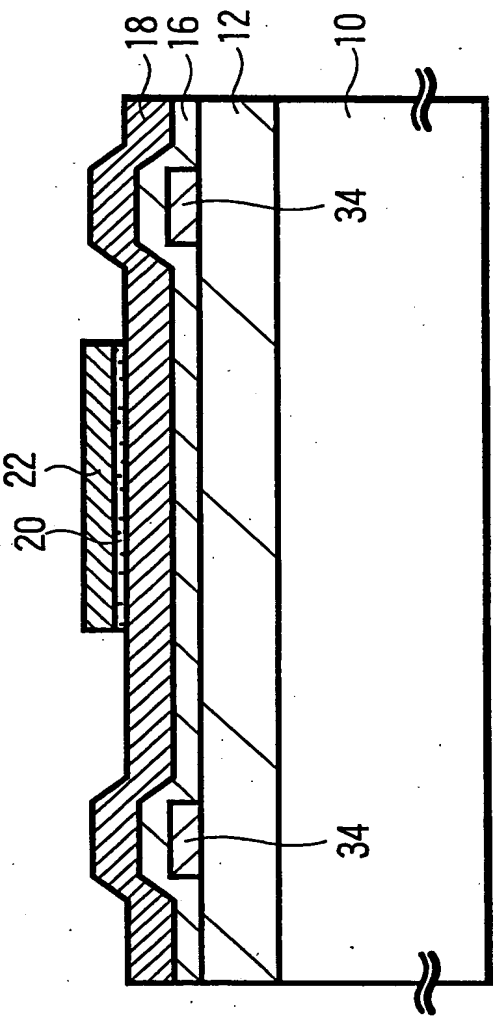

FIG. 34

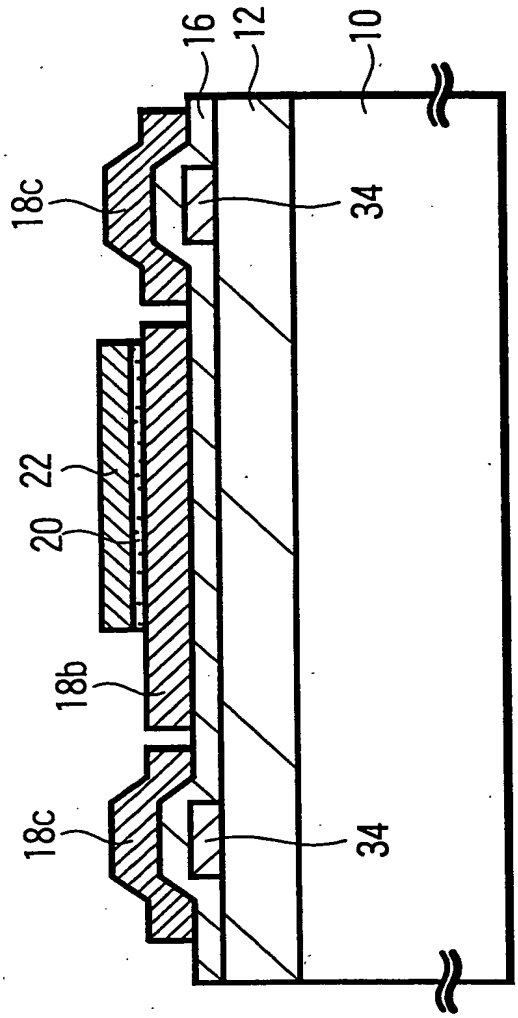
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FIG. 35

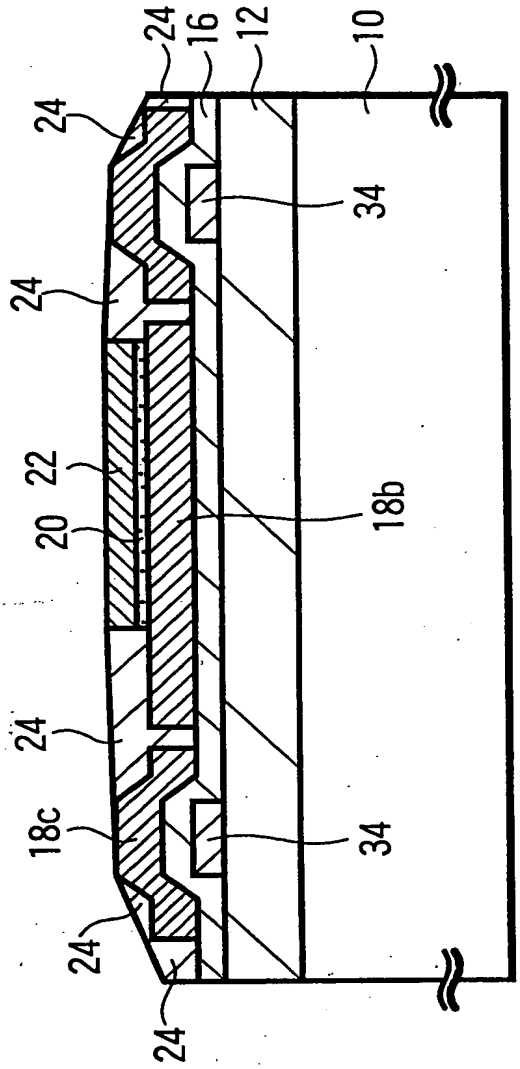
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FIG. 36

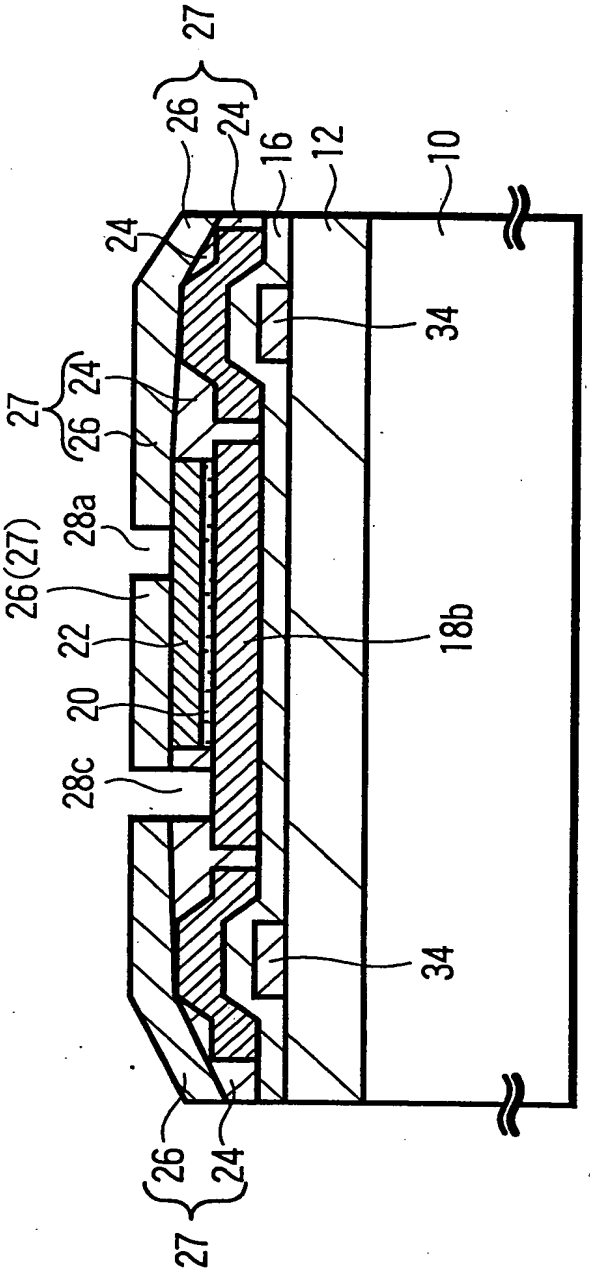
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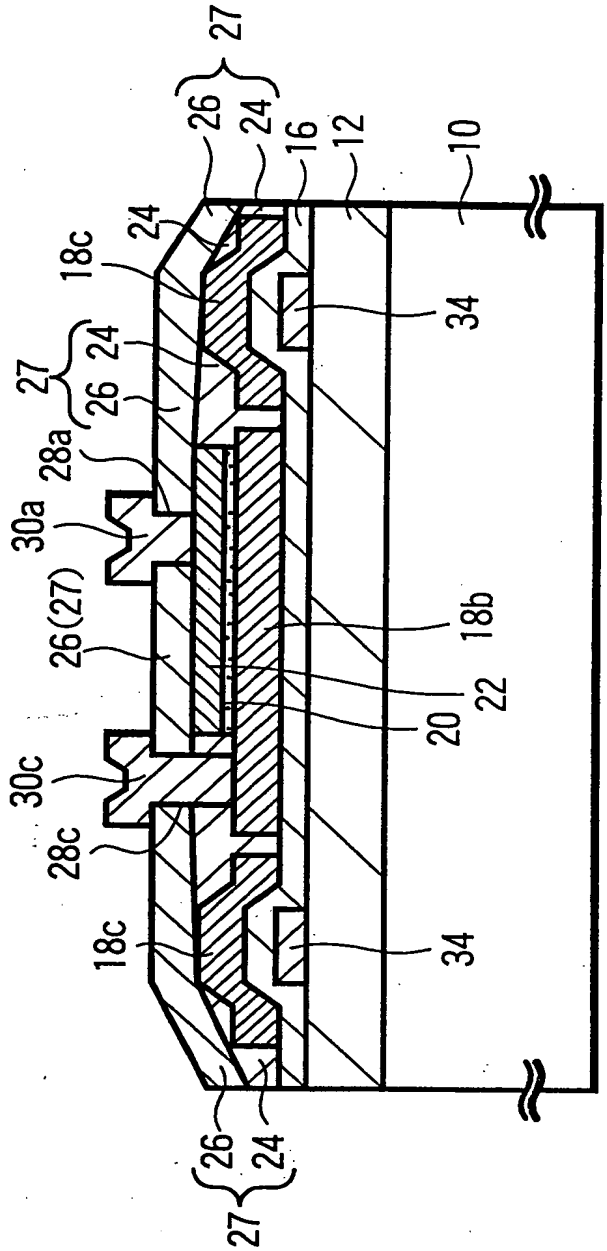
FIG. 37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28c
18c
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FIG. 38

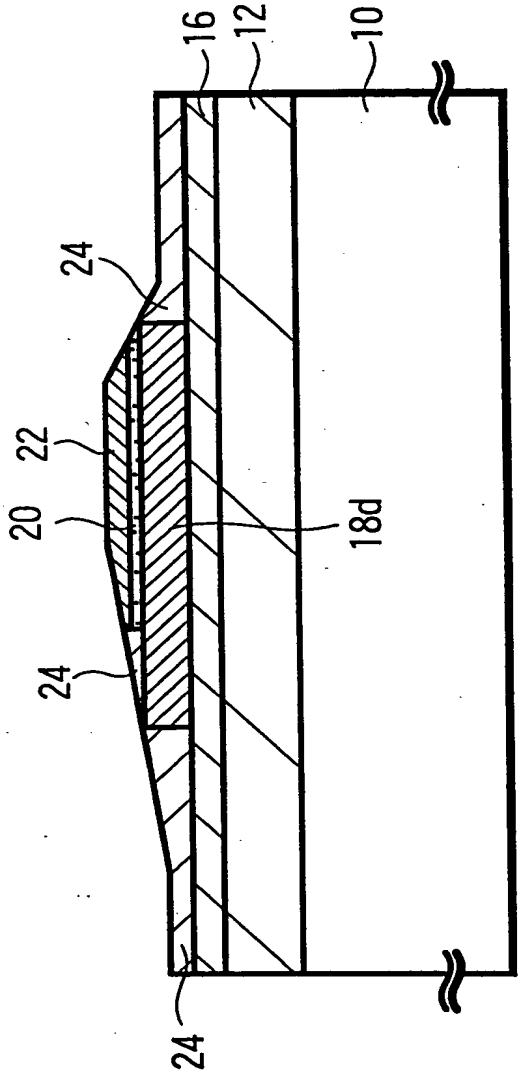
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FIG. 39

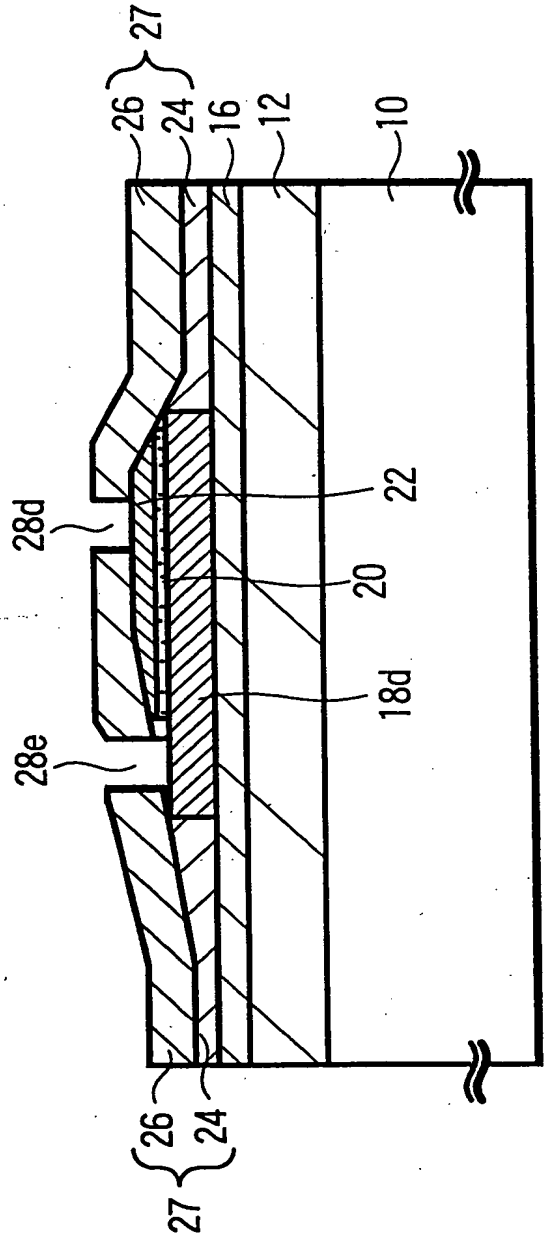
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FIG. 40

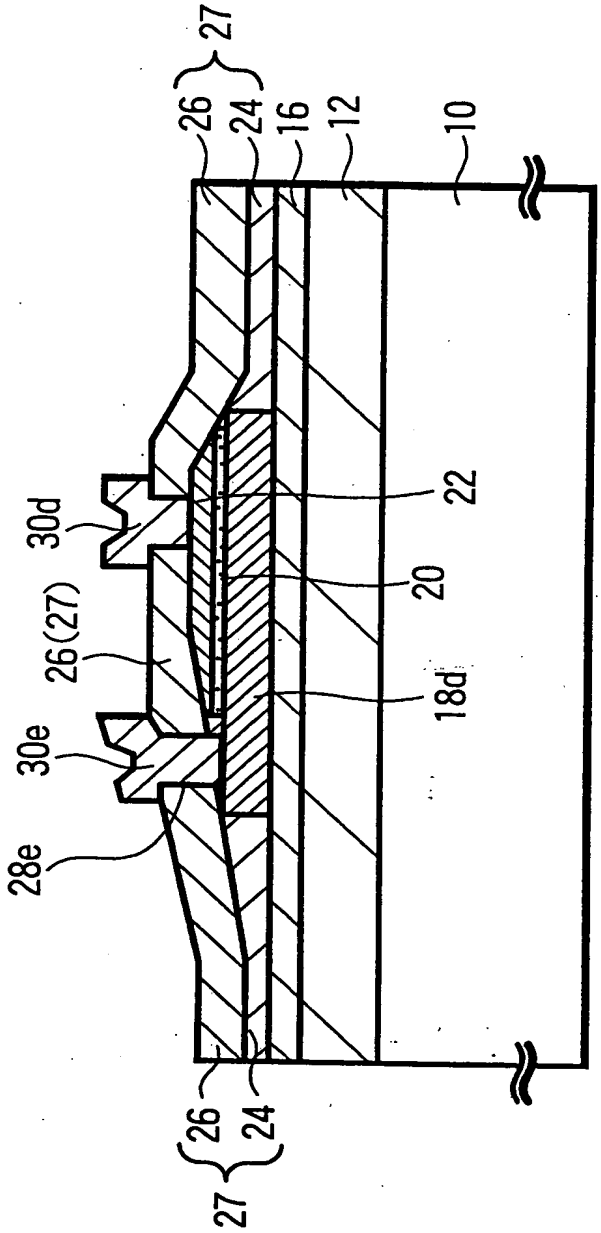

FIG. 41

DESCRIPTION OF REFERENCE NUMERALS

10 ... Semiconductor Substrate

12 ... The First Insulation Film

14 ... Polysilicon Dummy Layer

16 ... The Second Insulation Film

18 ... TiN/Al-Si/Ti/TiON/Ti Lamination film

18a, 18b, 18d ... Lower Electrode

18c ... Dummy Electrode

20 ... Dielectric Film

22 ... Upper Electrode

24 ... Smoothing Insulation Film

26 ... Insulation Film

27 ... Inter-layer Insulation Film

28a, 28d ... The First Via-hole

28b, 28c, 28e ... The Second Via-hole

30a, 30b ... The First Upper-layer Wiring Layer

30b, 30c, 30e ... The Second Upper-layer Wiring Layer

32 ... Insulation Dummy Layer

34 ... Polysilicon Dummy Layer